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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,176	03/02/2004	Kenichi Iizuka	108273-00006	3546

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EXAMINER	
VIDWAN, JASJIT S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,176	IIZUKA ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) ~~1-10~~ 1-29 is/are pending in the application.

4a) Of the above claim(s) 11-29 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/2/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group 1, Claims 1-10 in the reply filed on 5/12/06 is acknowledged. Non-elected claims 11-29 are withdrawn from consideration. Applicant is requested to cancel the non-elected claims from the present Application.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claim 3 recites the limitation "said buffers" in line 3. There is insufficient antecedent basis for this limitation in the claim. It is unclear to the Examiner to which "said buffer" the Applicant is referring to; i.e. whether 'said buffers' are in reference to the two buffers used to store and transmit data from Device 1 and 2 or to plurality of buffer areas inside individual buffer. For the purpose of the examination, Examiner will construe "said buffers" to be in reference to "plurality of buffer areas".

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 2, 3, 4, 5, 6, 7, 8, 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Preiss et al, U.S. Patent No: 6,757,763 [herein after Preiss].

3. **As per claims 1, 6 and 7**, Preiss teaches an information-processing unit **[Fig. 1, element 100]** for carrying out information processing in cooperation with an external host **[Fig. 1, element 103]** apparatus connected thereto via an external connection bus **[Fig. 1, element 107]**, comprising:

a. Internal CPU **[Fig. 1, element 102, "UDC"]**

b. Receive buffer for storing receive data received from said external host apparatus **[Fig. 2b, element 800, "8-Byte Receive FIFO"]**

c. Receive register for storing receive communication control information (Col. 3, Lines 51-52, "data") concerning the receive data **[Fig. 2b, element 806, "receiver register"]**

d. Transmit buffer for storing transmit data transmitted from said internal CPU via an internal bus **[Fig. 2b, element 300]**

e. Transmit register for storing transmit communication control information concerning the transmit data **[Fig. 2b, element 308, "transmit register"]**

f. Control circuit **[Fig. 1, 105, "EPEC"]** for passing the receive data stored in said receive register to said internal CPU and passing the receive communication control information stored in said receive register to said internal CPU **[Col. 3, Line 50 – Col. 4, Line 16, 'IN Transaction (Device to host)]**, and further passing the transmit data stored in said transmit buffer to said external host apparatus and passing transmit communication control information stored in said transmit register to said external host apparatus **[Col. 4, Lines 17-54, "Out Transaction (Host to Device)]**.

4. **As per claim 2**, Preiss teaches an inter-bus communication interface device wherein said buffer is of a type that outputs data in the order that the data are stored **[Col. 1, Lines 35-40, "FIFO –First in First Out"]**.

5. **As per claim 3**, Preiss teaches an inter-bus communication interface device wherein said buffer includes a plurality of buffer areas, said buffer areas being alternately [As data moves

across buffer areas, the location the data is stored will be alternately changed through the buffer] used in storing the communication data **[Col. 2, Lines 50-56]**.

6. **As per claim 4**, Preiss teaches communication interface device wherein said control circuit outputs an interrupt signal to the second device immediately after the communication control information is stored in said register **[Col. 3, Lines 1-8]**.

7. **As per claim 5 and 9**, Preiss teaches communication interface device further including a status register for storing information indicative of whether or not un-transmitted data exists in said register **[Col. 5 Lines 26-35]** and wherein said control circuit updates the information in said status register, when new data is stored in said register, or when data in said buffer is read out by the second device **[Col. 5, Lines 41-45]**.

8. **As per claim 8**, Preiss teaches information processing unit wherein said control circuit outputs an interrupt signal to said internal CPU, when said receive buffer is full of the receive data, or when the receive communication control information is stored in said receive register **[Col. 5, Lines 26-35]**.

9. **As per claim 10**, Preiss teaches information processing unit wherein said control circuit outputs a transmit data-related request signal for requesting reception of the transmit data, to said external host apparatus, when data is stored in said transmit buffer or said transmit register **[Col. 3, Lines 51-59]**.

References Cited Not Used

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Klingman, U.S. Patent No: 4954983 teaches two bus system wherein the data is transferred using buffers between internal bus (computer) and external device (Peripheral Device)

b. Shah et al, U.S. Patent No: 5,535,341 teach again two-bus system wherein the data is transfer-using buffers between internal and external bus.

c. Yazawa, U.S. Pub No: 2002/0078468 teaches a method of data transfer using a buffer and register to store information regarding the data stored in the buffer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
5/27/06

KIM HUYNH
SUPERVISORY PATENT EXAMINER
6/9/06